R09

Code No: D0601

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech II - Semester Examinations March/April 2011
ADVANCED COMPUTER ARCHITECTURE
(DIGITAL SYSTEMS & COMPUTER ELECTRONICS)

Time: 3hours **Max.Marks:60**

Answer any five questions
All questions carry equal marks

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1. a) Explain in detail a typical register organization of the CPU.
   b) Explain the terms – instruction format, instruction set, operands and addressing modes. [6+6]

2. a) Explain segmented – page mapping with an example.
   b) Explain about various mapping procedures in the organization of cache memory. [6+6]

3. a) A magnetic disk has the following parameters:
   T_s = Average time to position the magnetic head over a track
   R = Rotation speed of disk in revolutions per second
   N_t = Number of bits per track
   N_s = Number of bits per sector
   Calculate the average time T_a that it will take to read one sector.
   b) A non pipeline system takes 50ns to process a task. The same task can be proceed in a six-segment pipeline with a clock cycle of 10ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speed up that can be achieved. [6+6]

4. a) Explain in detail micro instruction sequencing and control.
   b) What are the problems in parallel processing? Explain various approaches for handling control hazards. [6+6]

5. a) Explain about interrupt driven IO.
   b) Explain about memory mapped IO and isolated IO. [6+6]

6. a) Explain the working of a CD-ROM.
   b) Explain in detail distributed shared memory. [6+6]

7. a) Explain VLIW approach for ILP.
   b) Explain multithreading and thread level parallelism. [6+6]

8. a) Explain in detail various RAID levels.
   b) Explain in detail practical issues in interconnecting networks. [6+6]

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